REMARKS

Claims 1-27 are pending in the application.

35 USC 112 Second Paragraph Rejection of Claims 31-33

The Office Action rejected claim 4 as allegedly being indefinite under 35 USC 112. In particular, claim 4 was rejected for allegedly lacking antecedent basis for the recited "said first half bridge segment" and "said second half bridge segment".

Claim 4 is canceled herein, making the rejection of claim 4 under 35 USC 112 now moot.

Claims 1-4, 9-14, 18-23 and 27 over Lange

In the Office Action, claims 1-4, 9-14, 18-23 and 27 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,457,091 to Lange et al. ("Lange"), with claims 6, 7, 15, 16, 24 and 25 rejected under 35 U.S.C. §103(a) as allegedly being obvious over Lange. The Applicants respectfully traverse the rejection.

Claims 1-4, 6, 7, 9-16, 18-25 and 27 recite a method and apparatus transferring data information between a first half bridge circuit and a second half bridge circuit over an LVDS connection.

Lange appears to rely on a high speed connector 112 to connect a first half bridge PCI circuit and a second half bridge PCI circuit (Fig. 4). The high speed connection is disclosed as being a serial gigabit Ethernet link (Lange, col. 4, lines 1-12).

Thus, Lange relies on Ethernet technology to transfer data from a first PCI buts to a second PCI bus. Gigabit Ethernet, at best, is able to communicate information at a rate of 1 Gb/s. The Applicants utilize a different technology that allows for higher transfer rates than Ethernet, i.e., an LVDS connection, as recited by claims 1-4, 6, 7, 9-16, 18-25 and 27.

An advantage of using LVDS versus Lange's use of Ethernet is, as disclosed in the Applicants' specification, e.g., speed and clock recovery. LVDS connections can attain speeds of up to 2.5 Gb/s while being able to communicate

clock and data within a serial bit stream. LVDS is a physical layer data interface standard defined by the TIA/EIA-644 and the IEEE 1596.3 standards. It is designed for high-speed, low-power, and low-noise point-to-point communications, typically over balanced, controlled-impedance media. LVDS radiates less noise than single-ended signals due to the canceling of magnetic fields, and is more immune to noise because it is coupled onto the two wires as a common-mode signal (i.e., equal levels of noise appear on both lines). Such advantages are not disclosed or suggested by Lange's disclosed use of Gigabit Ethernet.

Accordingly, for at least all the above reasons, claims 1-4, 6, 7, 9-16, 18-25 and 27 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 1-27 over Nakamura

In the Office Action, claims 1-4, 6, 8-13, 15, 17-22, 24, 26 and 27 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,606,6798 to Nakamura ("Nakamura"), with claims 5, 7, 14, 16, 23 and 25 rejected under 35 U.S.C. §103(a) as allegedly obvious over Nakamura. The Applicants respectfully traverse the rejection.

Claims 1-27 recite a method and apparatus wherein a first bus segment and a second bus segment that are connected to a common backplane have data transferred therebetween over an LVDS connection.

Nakamura is relied on by the Office Action to disclose a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment (Office Action, page 4). However, Nakamura appears to disclose the first bus segment is within a PC body 100 and a second bus segment is within a docking station 200 (Fig. 1). Nakamura fails to disclose or suggest connecting a first bus segment and a second bus segment connected to a common backplane, mush less use of an LVDS connection to do so, as recited by claims 1-27.

Nakamura is addressing a completely different problem within the art, i.e., maintaining a high speed connection between a PC body and a docking station. Wherein, Applicants are addressing a problem within the art, as discussed in the background of the invention, with reducing latency between multiple bus segments connected to a common backplane. As Applicants discuss, latency within a common backplane connecting multiple bus segments has a negative impact on time sensitive applications, such as telecommunications. With a common backplane carrying telecommunication information, latency between bus segments can be perceived as pauses and gaps within a telephone conversation. Applicants address such deficiencies within the art of connecting bus segments connected to a common backplane through use of an LVDS connection. Such a use of an LVDS connection is not disclosed or suggested by the cited prior art.

Accordingly, for at least all the above reasons, claims 1-27 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,
MANELLI DENISON & SELTER PLLC

William H. Bollman
Reg. No.: 36,457
Tel. (202) 261-1020
Fax. (202) 887-0336

2000 M Street, N.W. 7th Floor
Washington D.C. 20036-3307
WHB/df